PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-274987
(43)Date of publication of application : 05.10.2001

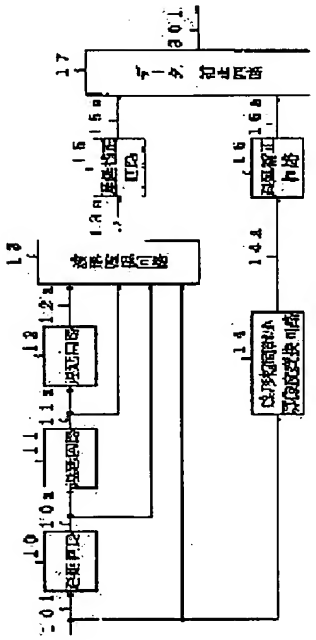
(51)Int.Cl. H04N 1/387
G06T 3/40
G09G 5/36
H04N 1/393

(21)Application number : 2000-088808
(22)Date of filing : 28.03.2000

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : YAMAUCHI TOSHIYUKI
TACHIKAWA KOJI
YAMAZAKI KOICHI

(54) IMAGE PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a clear image which is approximate to its original by preventing the deterioration of sharpness or the uneven luminance that is caused when the resolution of a digital image is converted.
SOLUTION: A linear interpolation reduction resolution converter 14 inputs a digital original image 101 to convert it into a digital reduced or enlarged image by the linear interpolation system and in response to a designated conversion rate and outputs a linear interpolation signal 14a. A waveform monitoring circuit 13 always monitors the levels of the image 101, a 1-step delay signal 10a, a 2-step delay signal 11a and a 3-step delay signal 12a respectively and detects the pixels of both top and bottom parts of each level. A data correction circuit 17 replaces a delay-corrected linear interpolation signal 16a with a delay- corrected correction pixel signal 15a and generates a reduced image 301.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2001－274987
（P2001－274987A）
(43)公開日　平成13年10月5日(2001.10.5)

(51)Int.Cl.⁷		識別記号	FI			テーマコード(参考)
H04N	1/387	101	H04N	1/387	101	5B057
G06T	3/40		G06T	3/40	C	5C076
					D	5C082
G09G	5/36		H04N	1/393		
H04N	1/393		G09G	5/36	520F	

審査請求　未請求　請求項の数４　ＯＬ　（全 10 頁）　最終頁に続く

(21)出願番号　特願2000－88808(P2000－88808)

(22)出願日　平成12年３月28日(2000.3.28)

(71)出願人　000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地

(72)発明者　山内　利之
香川県高松市古新町８番地の１　松下寿電子工業株式会社内

(72)発明者　立川　浩司
香川県高松市古新町８番地の１　松下寿電子工業株式会社内

(74)代理人　100084364
弁理士　岡本　宜喜

最終頁に続く

(54)【発明の名称】　画像処理装置

(57)【要約】
【課題】　ディジタル画像を解像度変換する際に、画像の先鋭度の劣化や輝度むらの発生を防ぎ、より原画に近い鮮明な画像を得ること。
【解決手段】　線形補間縮小解像度変換回路１４はディジタル原画像１０１を入力し、指定された変換倍率に応じて線形補間方式を用いてディジタル縮小又は拡大画像に変換し、線形補間信号１４ａを出力する。波形監視回路１３はディジタル原画像１０１、１段遅延信号１０ａ、２段遅延信号１１ａ、３段遅延信号１２の各レベルを常時監視し、そのレベルの山頂部分と谷底部分の画素を検出する。データ補正回路１７は遅延補正された線形補間信号１６ａを、遅延補正された補正画素信号１５ａで置き換え、縮小画像３０１を生成する。